

REMARKS

In the previous office action, Claims 1-10 were examined and rejected. No claims are amended, no claims are added; no claims are canceled. Applicant respectfully requests reconsideration of Claims 1-10 in view of at least in the following.

I. Claims Rejected Under 35 U.S.C. §103

The Patent Office rejects Claims 1-10 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,696,732 to Matsuoka, et al. ("Matsuoka") and U.S. Patent No. 5,541,427 to Chappell, et al. ("Chappell") and U.S. Patent No. 5,348,899 to Dennison, et al. ("Dennison"). To render a claim obvious, all elements of that claim must be taught or suggested by at least one properly combined reference.

Applicant respectfully disagrees with the rejection above and submits that independent Claim 1 is allowable for at least the reason that the cited references do teach or suggest a contact extending a first depth through a first thickness of a dielectric layer to a gate, and extending a different second depth through a portion of a second thickness greater than the first thickness, short of the junction region as required by Claim 1. According to Claim 1, for example, a contact may extend through a first thickness of a dielectric to contact a gate, and extend deeper into a second thickness of the dielectric over a junction region adjacent to the gate short of the junction region (e.g., **Figures 3-4 and 12-13**). Similarly, the contact may extend into the thicker thickness of dielectric adjacent to the gate, to a lesser depth than the first thickness (e.g., see **Figures 6 and 9**).

Matsuoka describes gated device 14c in an SRAM cell having first and fourth contacts 44, 46 which either go through the dielectric layer and either stop at the etch stops or go to the gate, or a junction region 14a, b (see **Figure 23** and col. 10, lines 9-35). First to fourth contacts 44 and 46, each extend only through one thickness of the dielectric. Specifically, Matsuoka teaches local wiring 24 embedded in a corresponding through hole 22 connecting gate electrode 14c and the source/drain region 14b of NMOS 14 with source/drain region 16a of PMOS 16 (see Figure 2 and column 6, lines 52-62).

On the other hand, Dennison teaches electrode 50 in a region etched through layers 46 and 44 with an etched timing such that silicide region 42 is reached with minimal over-etch such that the adjacent substrate is not reached (see column 5, lines 27-31 and Figures 2-3). Hence, combining contact 50 of Dennison with local wiring 24 of Matsuoka would render local wiring 24 of Matsuoka improper for its intended purpose of connecting gate electrode 14c, source drain region 14b and source drain region 16a, because electrode 50 is not allowed to reach the adjacent substrate and thus would not contact region 14b or 16a. (See MPEP § 2145.X). Similarly, the combination would render electrode 50 unsatisfactory for its intended purpose of not reaching the substrate, if electrode 50 were combined with wiring 24, because wiring 24 must reach the substrate to connect electrode 14c, region 14b, and region 16a. (See MPEP § 2145.X). Hence, for at least this reason, Applicant respectfully requests the Patent Office withdraw the rejection of above claim 1.

Applicant submits that dependent claims 2-10, being dependent upon allowable base Claim 1, are patentable over the cited reference for at least the reasons explained

above. Thus, Applicant respectfully requests that the Patent Office withdraw the rejection of dependent claims 2-10 noted above.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record and are in condition for allowance, and such action is earnestly solicited at the earliest possible date.

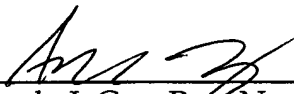
If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17. If a telephone interview would expedite the prosecution of this Application, the Examiner is invited to contact the undersigned at (310) 207-3800.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to:
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Andrea Costello Date